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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/086,494	03/01/2002	Donald Charles Soltis JR.	10016692-1	2136

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EXAMINER	
ROSS, JOHN M	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 02/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/086,494	SOLTIS, DONALD CHARLES	
	Examiner	Art Unit	
	John M Ross	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *31-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *31-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 18 November 2004 has been entered.

Status of Claims

2. Claims 1-30 are canceled.

Claims 31-50 are new.

Claims 31-50 are rejected.

Response to Amendment

3. Applicant's amendment filed on 18 November 2004 in response to the office action mailed on 19 October 2004 necessitates new ground(s) of rejection as presented below in this Office action.

Information Disclosure Statement

4. The Information Disclosure Statement(s) received 18 November 2004 has been considered. Please see attached PTO-1449(s).

Claim Objections

5. Claims 34 and 44 are objected to because of the following informalities:

Lines 7-10 of claim 34 should be amended as follows:

the first mapping maps to different cache units than the ~~second~~ third mapping, and the ~~third~~ second mapping maps to different partitions than the fourth mapping.

Claim 44 contains similar deficiencies and should be corrected accordingly.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claim 31-38 and 40-50 are rejected under 35 U.S.C. 102(b) as being anticipated by Brenza (US 4,905,141).

As in claim 31, Brenza discloses a system comprising:

a plurality of processors (Fig. 2, elements 70, 72, 74, 76, 80, 82, 84, 86, 88, 90, 92, 94, 96 and 98; column 6, line 46 to column 7, line 2), where the plurality of processing elements comprising the CPU of Brenza are viewed as processors because they receive instructions, generate addresses, fetch and store data from memory, and operate on data (see also column 3, lines 19-34);

a plurality of cache units (Column 3, lines 35-39 and 51-53; Fig. 2, element 50; column 6, lines 1-4; column 7, lines 46-50);

a crossbar interface between the plurality of processors and the plurality of cache units (Column 3, lines 53-59; Fig. 2, elements 52 and 58; column 7, lines 50-55), where it is noted that the switches of Brenza as described are functionally equivalent to a crossbar switch;

a plurality of tables for the plurality of processors (Fig. 2, elements 100, 102, 104, 106 and 108; column 6, lines 64-67);

each table identifying

which of the plurality of cache units are available to the corresponding processor (Column 3, lines 47-50; column 4, lines 1-9; column 7, lines 12-19; Figs. 9 and 10; column 13, lines 32-54); and

which of a plurality of memory partitions are available to the identified cache units (Column 13, lines 55-64), where the zone identifier disclosed by Brenza inherently identifies a main memory partitioned according to ranges of addresses because Brenza

explicitly states that the zone partitioning conforms to that taught by Bean et al in US Pat. No. 4,843,541, which shows a main memory partitioned into a plurality of address ranges (See Fig. 1 of Bean).

As in claim 32, partitions representing non-overlapping main memory address ranges are inherent in Brenza by the same reasoning given in the rejection of claim 31 (See Fig. 1 of Bean).

Claim 33 is rejected using the same rationale as for the rejection of claim 31, noting that there is no requirement or expectation that the PLATs as taught by Brenza would be symmetrical, and in fact it would be expected that the data contained therein would differ from table to table.

Claims 34-38 are rejected using the same rationale as for the rejection of claim 33 according to the following reasoning: Brenza teaches PLATs mapping between a zone partition (i.e. memory partition corresponding to an address range), a cache partition and a memory address for each processor (Figs. 9 and 10; column 13, lines 32-64). The system of Brenza is completely flexible in that any processor can access any cache partition and any address associated with any zone identifier (Column 7, lines 50-55; column 8, lines 7-12; column 13, lines 55-64). Therefore, it is understood in Brenza that different tables will simultaneously describe mappings to both of the same and different cache and memory partitions as recited in claims 34-36. Furthermore, there is no requirement or expectation in Brenza that all of the cache partitions and all of the memory partitions be mapped to a particular processor as recited in

claims 37-38. In fact, Brenza teaches a miss in the PLAT which means that no cache partition or memory partition is mapped to the processor (Column 8, lines 13-21).

Claim 40 is rejected using the same rationale as for the rejection of claim 31, noting that Brenza teaches a dynamic system where the PLATs are updated (Column 8, lines 7-21).

Claims 41-48 are rejected using the same rationale as for the rejection of claims 31-38 as above.

Claim 49 is rejected using the same rationale as for the rejection of claim 40 above.

Claim 50 is rejected using the same rationale as for the rejection of claim 31.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over Brenza (US 4,905,141) in view of Olukotun (Kunle Olukotun et al, "The Case for a Single-Chip Multiprocessor", Proceedings of the Seventh International Conference on Architectural Support for Programming Languages and Operating Systems, Cambridge, MA, Oct. 1996).

Brenza is relied upon for the teachings relative to claim 31 as above.

Brenza does not teach that the plurality of processors, plurality of cache units, crossbar and plurality of tables are configured on a single die as required by claim 39.

Olukotun teaches a single-chip multiprocessor comprising a crossbar-connected shared L2 cache located on the same die as the processors (Fig. 3; § 4.2). Olukotun teaches that increasing integration density allows for higher clock rates, allowing microprocessor performance growth (§ 1, paragraph 1).

Regarding claim 39, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to integrate the elements taught by Brenza on the same die as taught by Olukotun, in order to allow for higher clock rates and performance growth as taught by Olukotun.

Response to Arguments

10. Applicant's arguments filed 18 November 2004 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John M Ross whose telephone number is (571) 272-4212. The examiner can normally be reached on M-F 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JMR

2/17/05

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER